Uncertainties of immunity measurements

DTI-NMSPU project R2.2b1

Annex F *Electronic circuit susceptibility investigation*

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ELMAC services

Annex F

Electronic circuit susceptibility

This annex describes the investigation of the RF susceptibility of analogue and digital electronic circuits. Two simple circuits, one analogue and one digital, are subjected to an unwanted applied RF signal and their response is noted. The unwanted signal is an unmodulated RF carrier across the frequency range 0.5MHz to 200MHz developed from a signal generator feeding an RF amplifier, and applied to the circuit via a broadband transformer. The level quoted in the results was pre-calibrated across frequency and refers to the voltage across points A-A in the circuit diagrams, in the absence of the ICs.

Test circuit: analogue

The analogue test circuit is a unity-gain op-amp in which the interfering RF signal is applied in series with the non-inverting input. The DC conditions of the op-amp can be modified as follows, depending on the intended supply rails of the type under test:

V+	+12V	+12V	+12V	+5V
V–	–12V	–12V	0V	0V
V_{out}	0V	0.9V	2.2V	2.2V

The circuit diagram of the op-amp test circuit is shown in Figure 1.

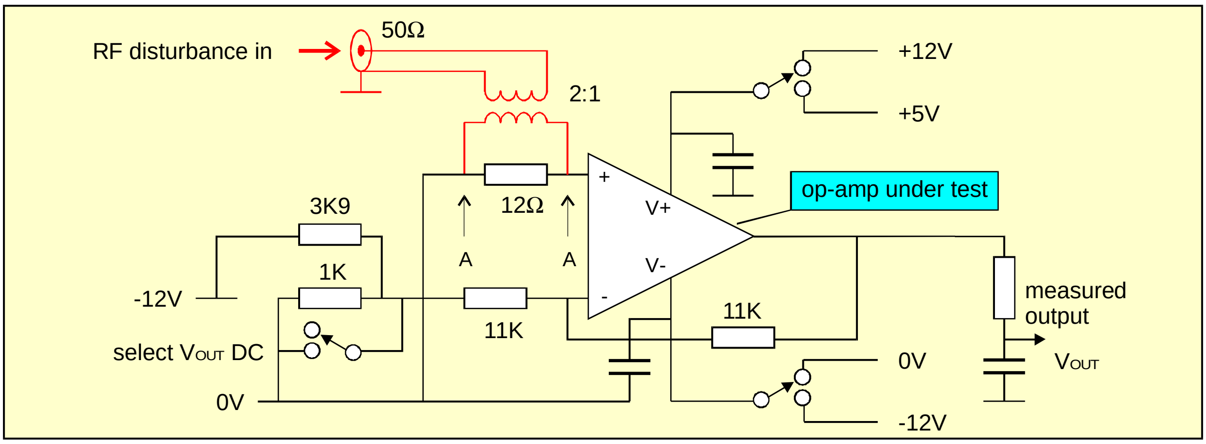


Figure 1 Op-amp analogue immunity test circuit

Single units of various types of op-amp device, selected mainly for availability, were tested, as follows:

Type	Technology
LM301A	Bipolar, dual supply, simple
NE5534	Bipolar, dual supply, complex
OP27	Bipolar, dual supply, complex
LM358N (Philips)	Bipolar, single supply, simple
LM358N (National)	
CA358 (Harris)	
TLC272	CMOS, single supply
CA3240	BiMOS, bipolar output, dual supply
CA3260	BiMOS, CMOS output, single supply

In some cases the devices were tested across the frequency range to determine their most susceptible frequencies. In all cases the devices were subjected to an increasing RF level at spot frequencies to determine their RF-to-output transfer function. The resulting data is shown in the next section. It shows the value of the deviation from the undisturbed level and does not take into account the DC output offset of +2.2V that is set up to represent typical operating conditions of single-supply circuits.

Results

- Different op-amp technologies have different characteristic functions;
- for a given type, different responses can be observed at different frequencies;
- the DC operating conditions often have a marked effect on the response, and this is particularly noticeable when single-supply devices are operated close to their lower common mode voltage limit;
- only one of the devices, the LM301A which has the oldest design, showed a response that was approaching linearity over the range tested. All others showed greater or lesser non-linearity.

Test circuit: digital

The digital test circuit is a series of inverting buffers feeding the clock and data inputs of a D-type flip-flop latch as shown in Figure 2. The buffers are driven from a 6MHz clock oscillator. The buffers are arranged such that there is a short delay, selectable by a link, between the rising clock edge (which clocks the level at the D input into the flip-flop) and the D input itself. Thus a change in the relative delay at these two inputs, due to the disturbing RF voltage, will cause an incorrect value to be latched into the flip-flop, resulting in an error in the output value. The filtered output voltage is monitored on a DVM and any departure from a constant high or low value (depending on the relative phase of clock and D input) represents a failure. The greater the voltage, the more the clock signal has been disturbed by the RF.

In practice, each individual clock cycle will be delayed by a different amount depending on the frequency relationship between it and the interfering signal. If the interference is very close to 6MHz or a multiple or sub-multiple thereof, beat signals are observed at the output; otherwise the difference frequency is attenuated by the output filter and is not observed on the voltmeter used for monitoring, although it could be on an oscilloscope.

The undisturbed output voltage will be either a logic high or low depending on the relative phases of CK and D inputs. The graphs shown in the following section are of the absolute difference voltage from the undisturbed state, which is therefore not sensitive to the phasing.

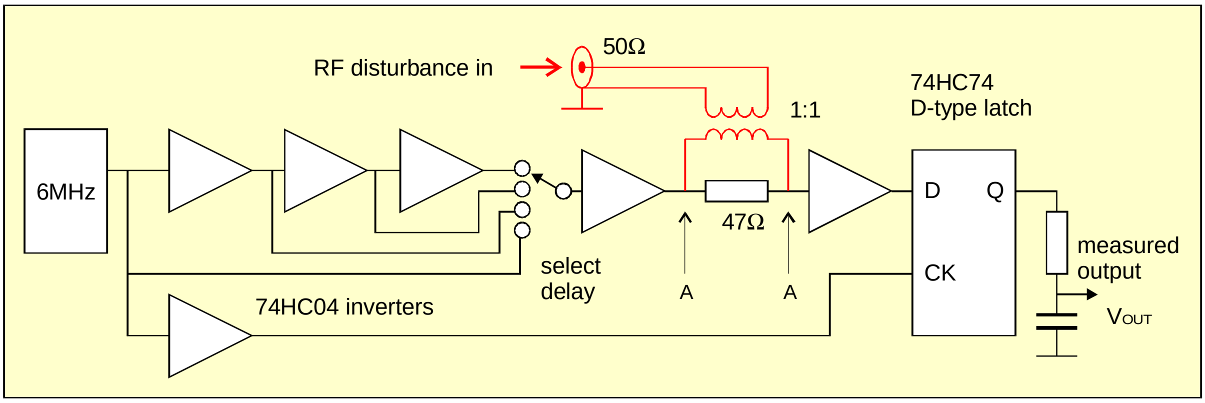


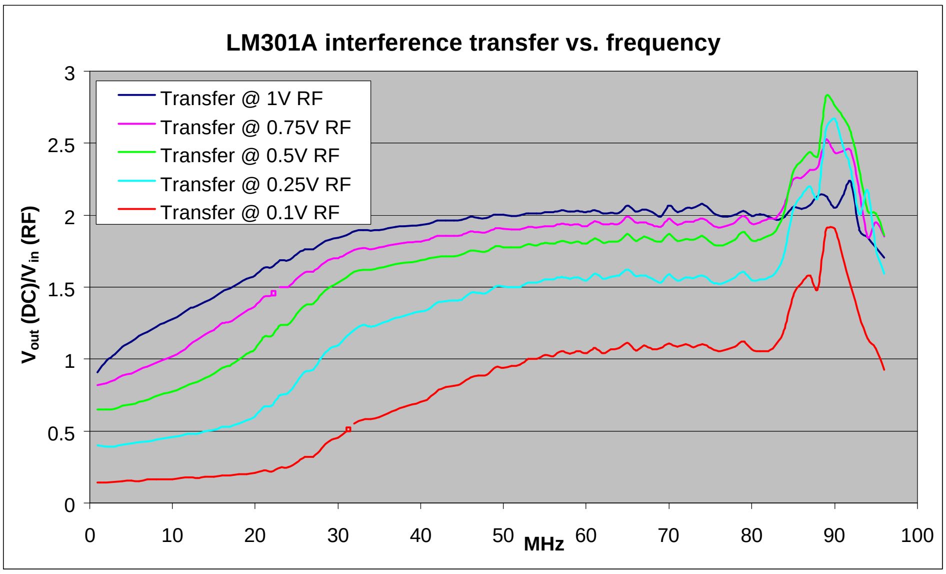
Figure 2 Digital immunity test circuit

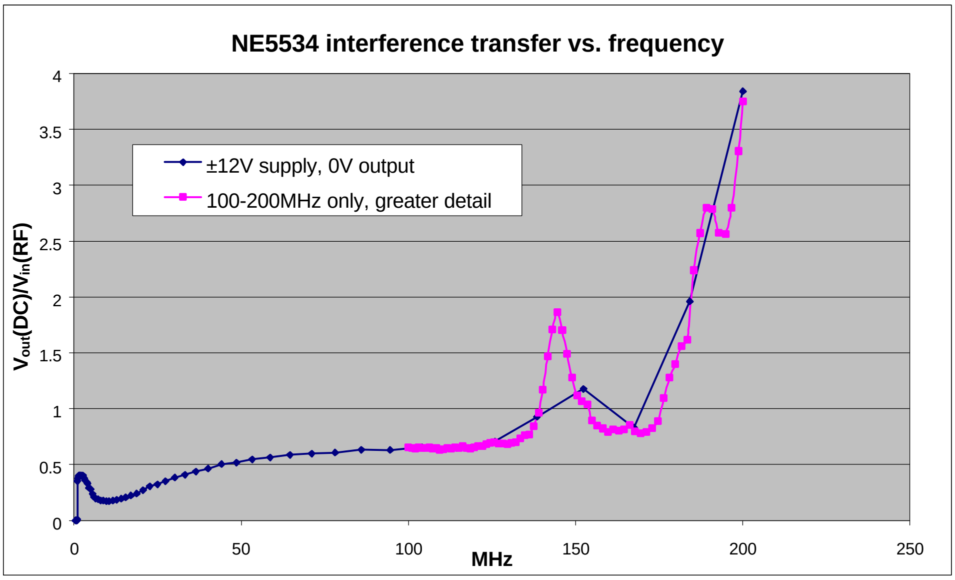
Results

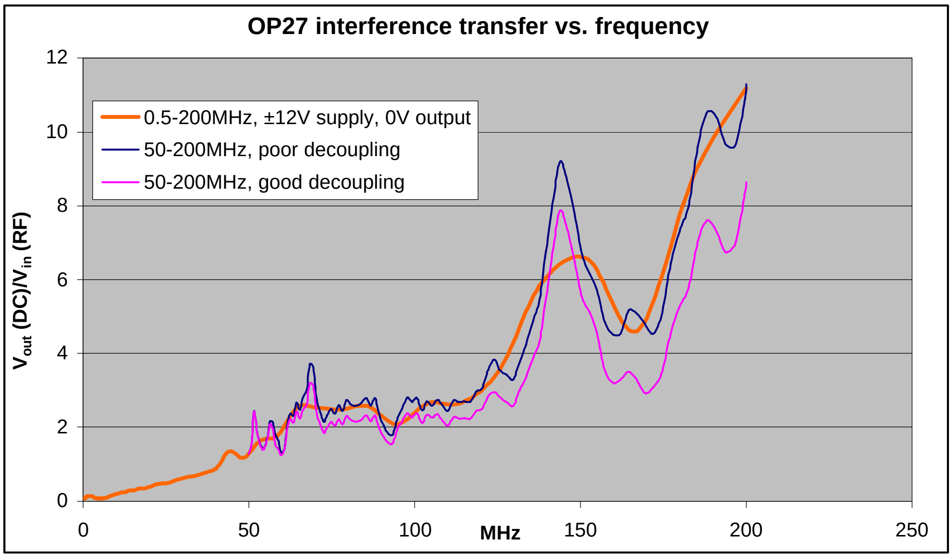
Absolutely no effect on the output voltage was observed up to some level dependent on frequency. Above this level a near-linear increasing deviation was observed.

Analogue circuit RF susceptibility data

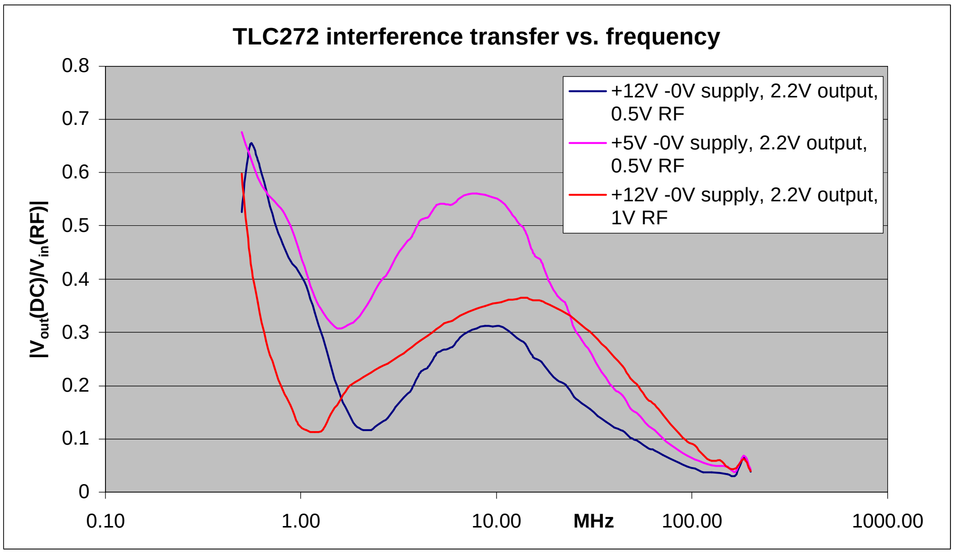
Interference transfer functions versus frequency (older bipolar types)

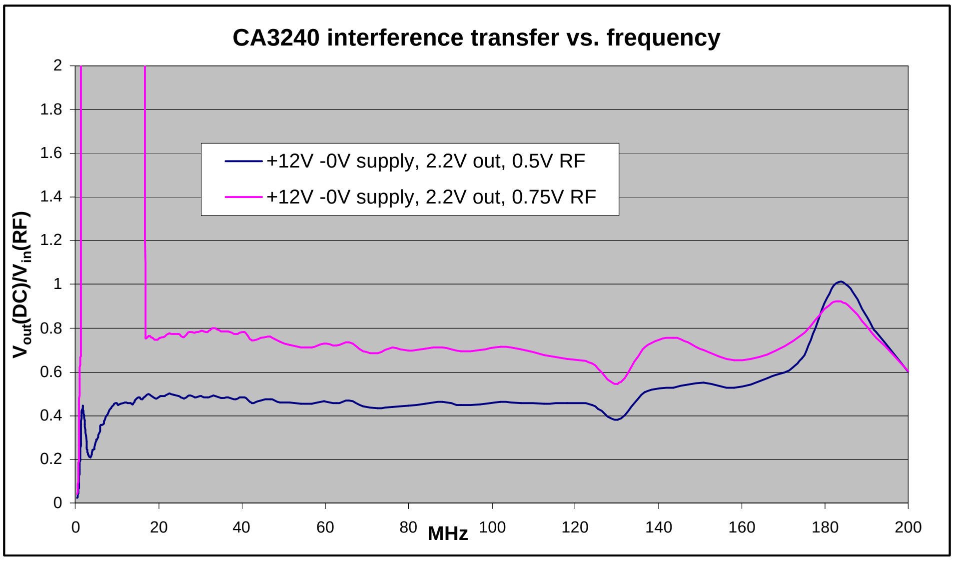


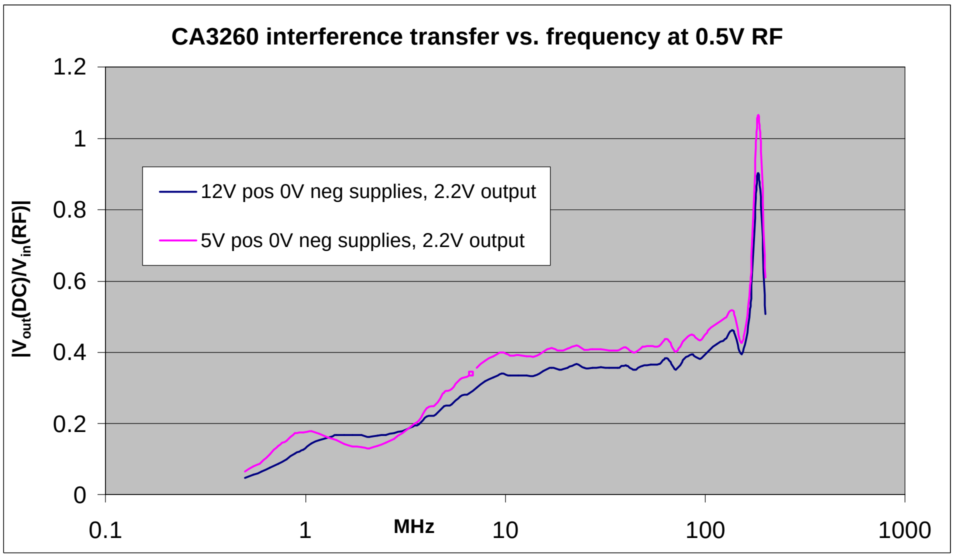




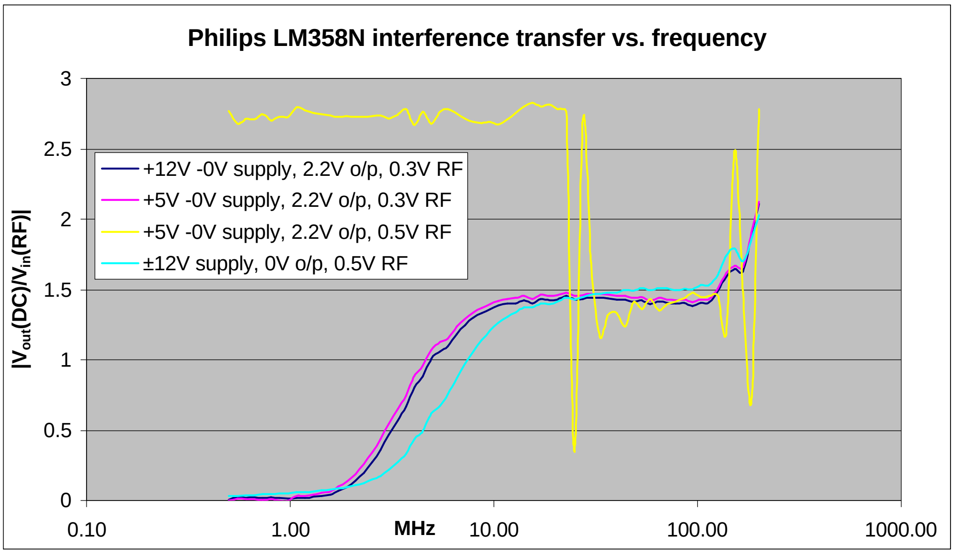
Interference transfer functions versus frequency (CMOS and Bi-MOS types)

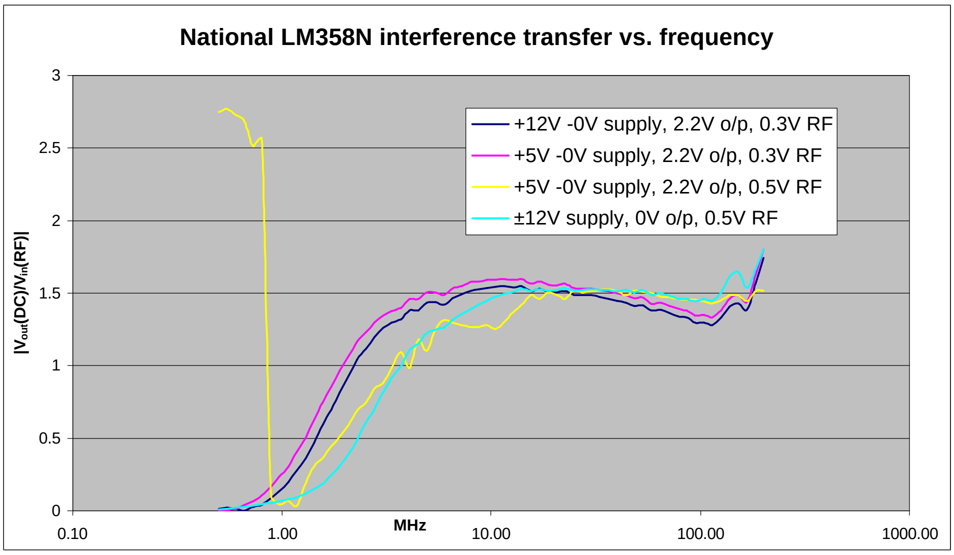


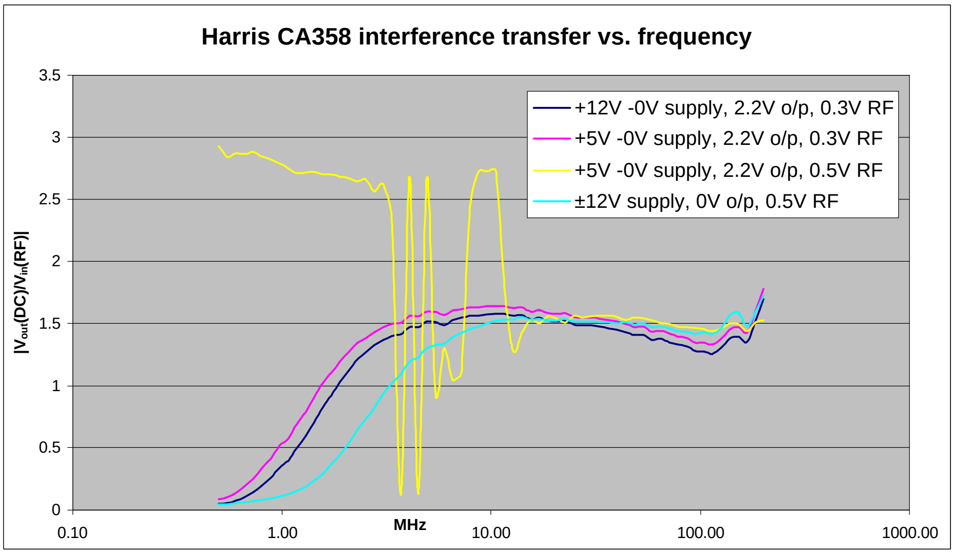




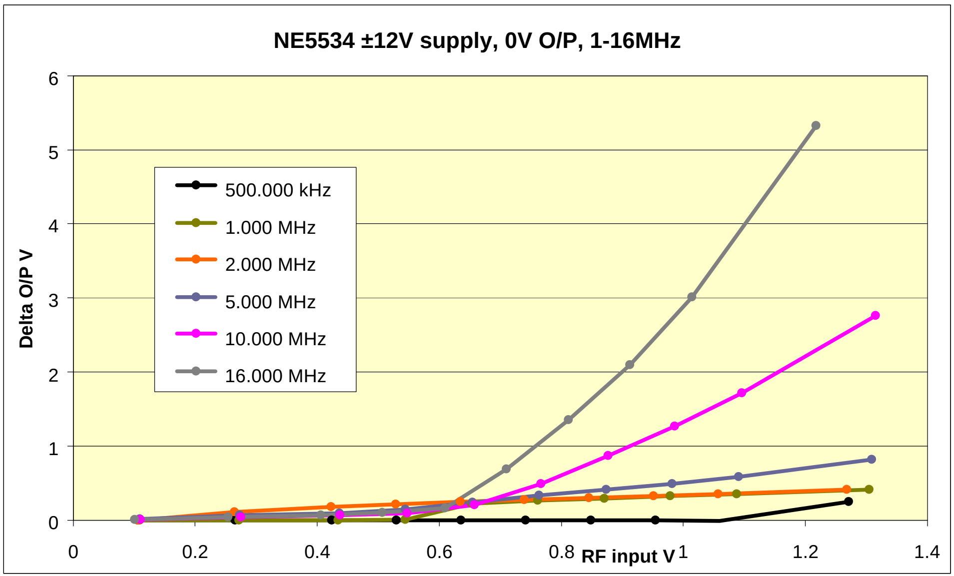
Interference transfer functions versus frequency (LM358 types)

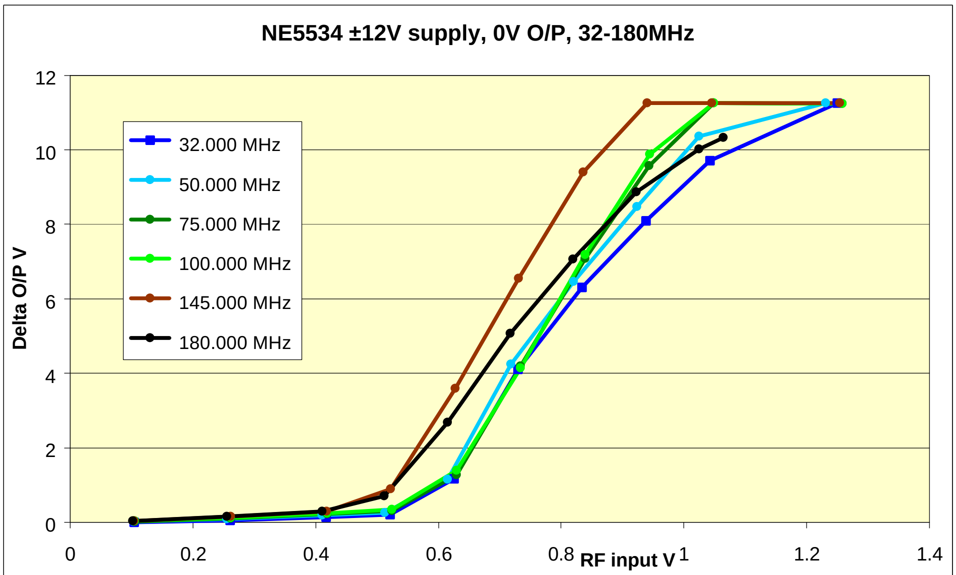


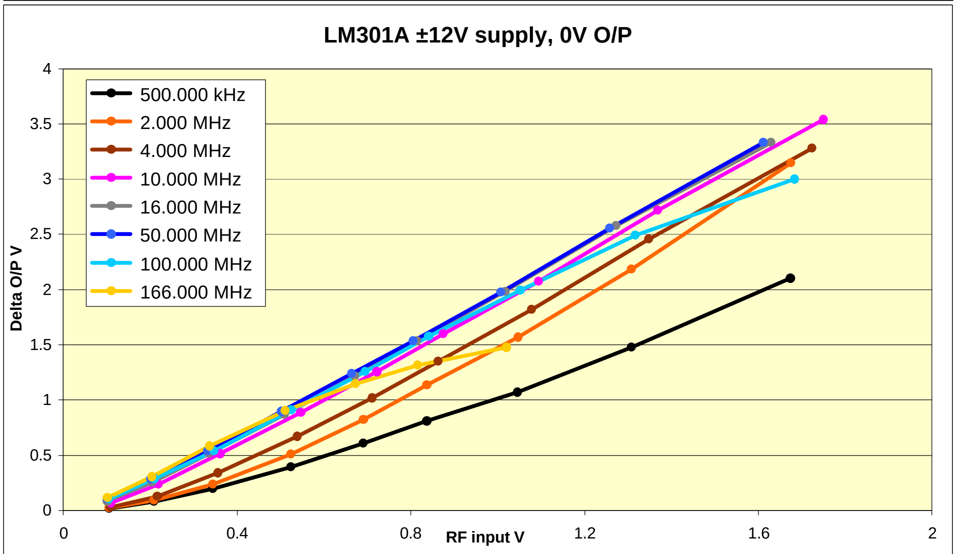




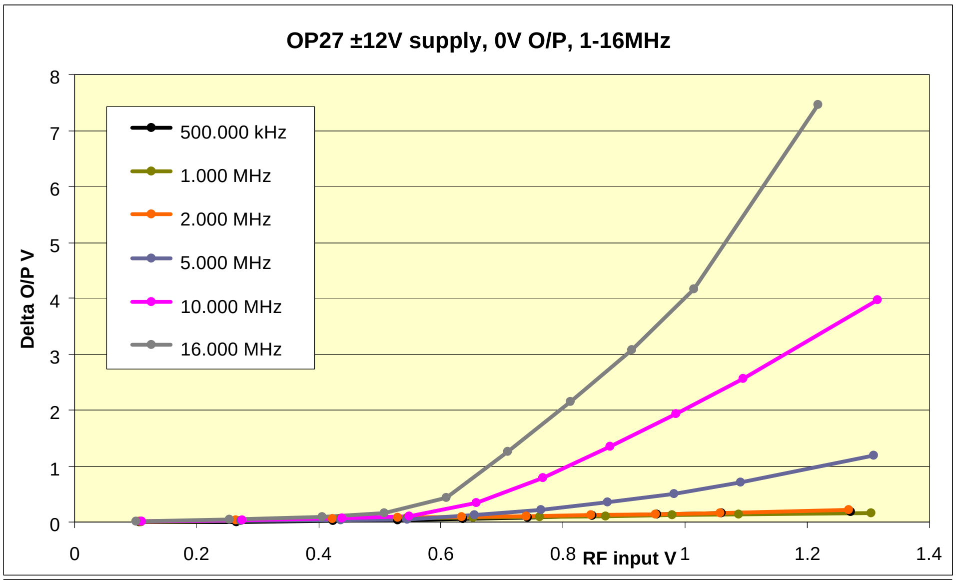
Interference transfer functions versus level

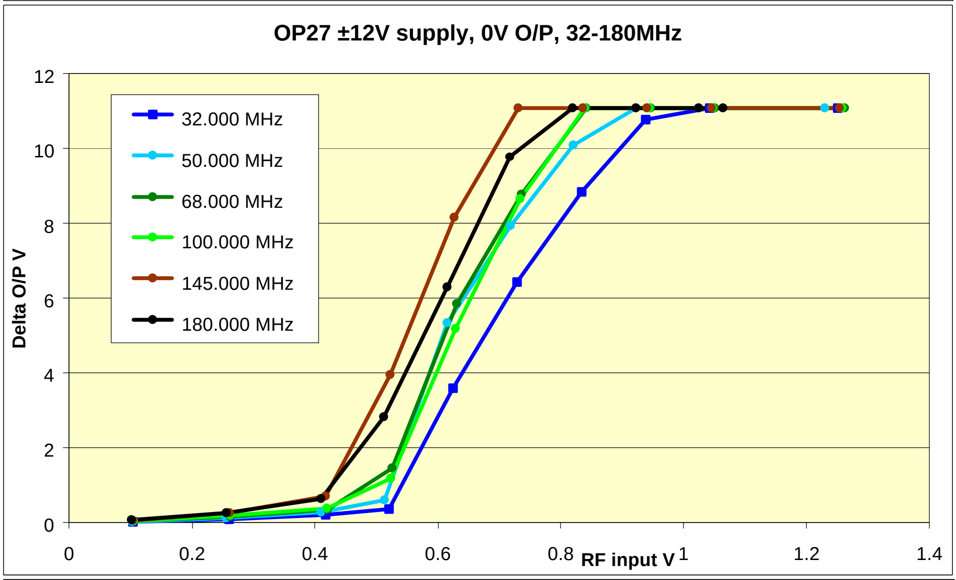


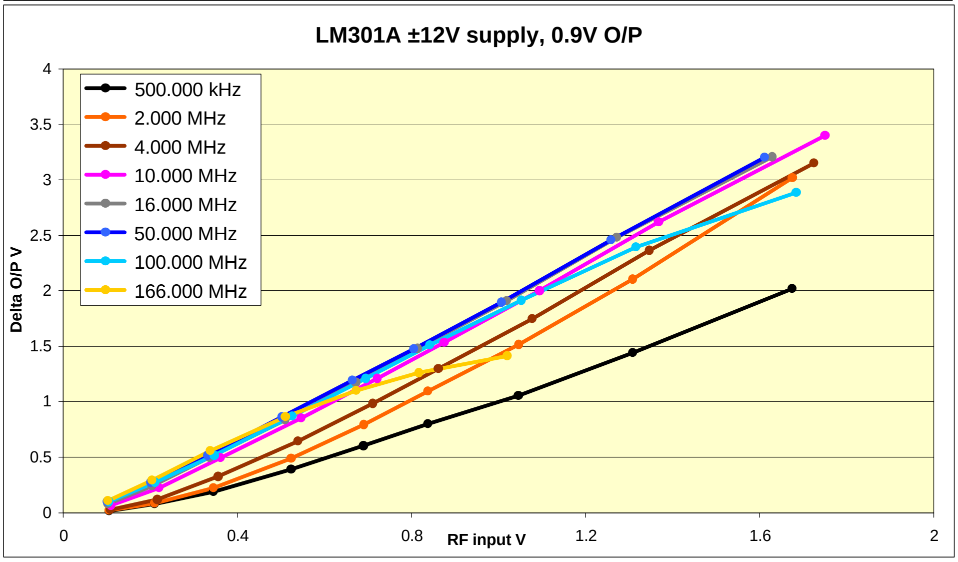




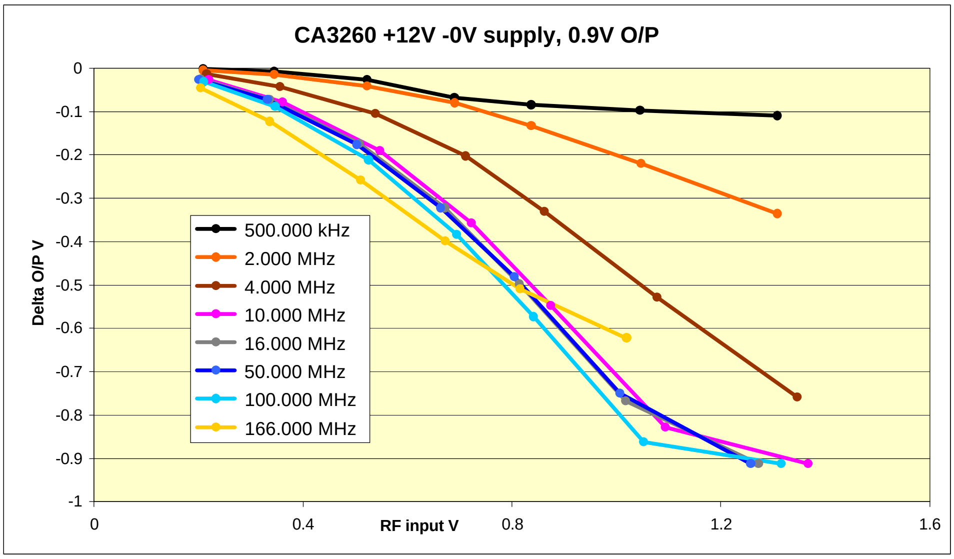
Interference transfer functions versus level (continued)

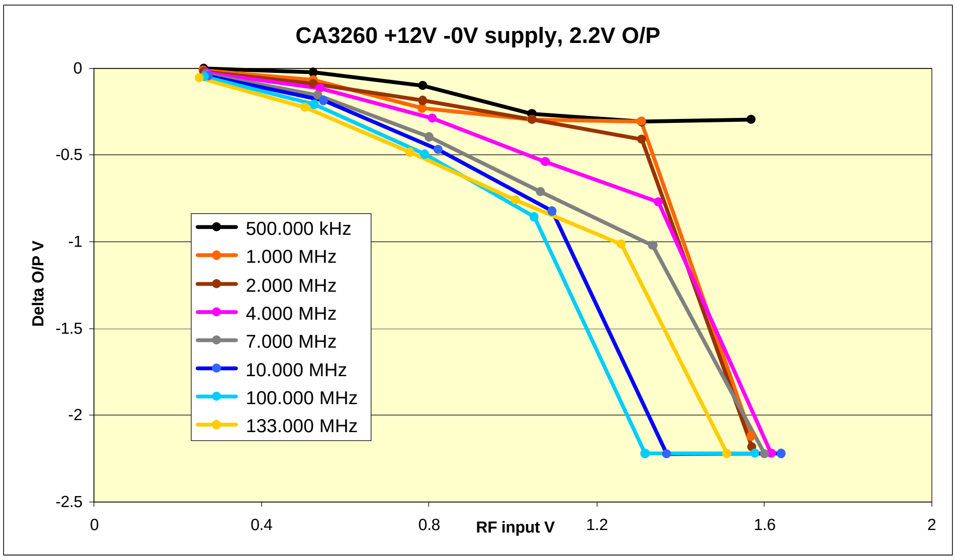


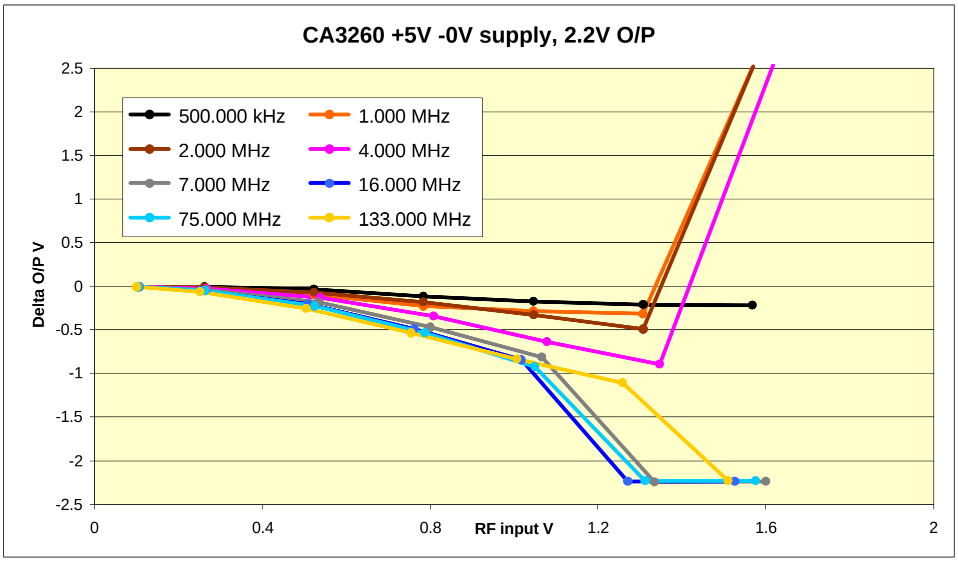




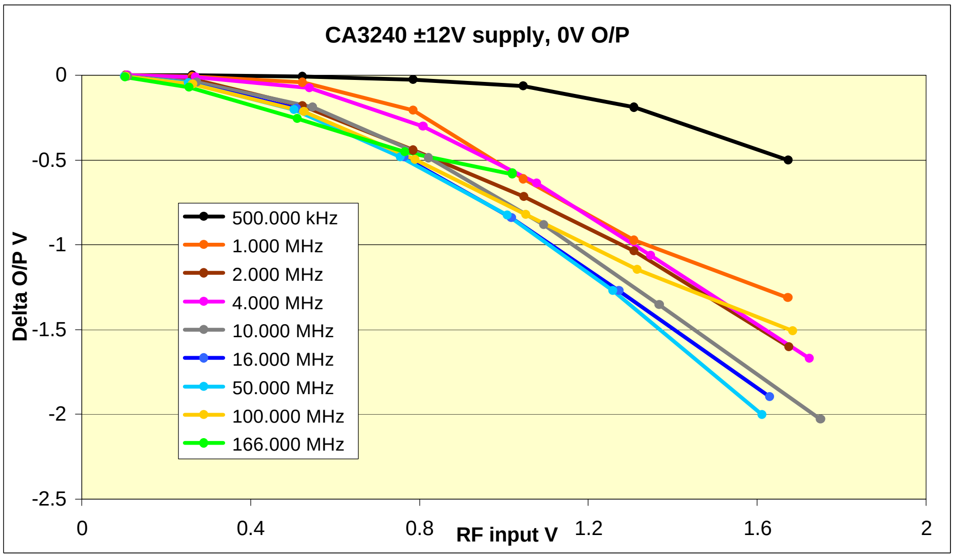
Interference transfer functions versus level (continued)

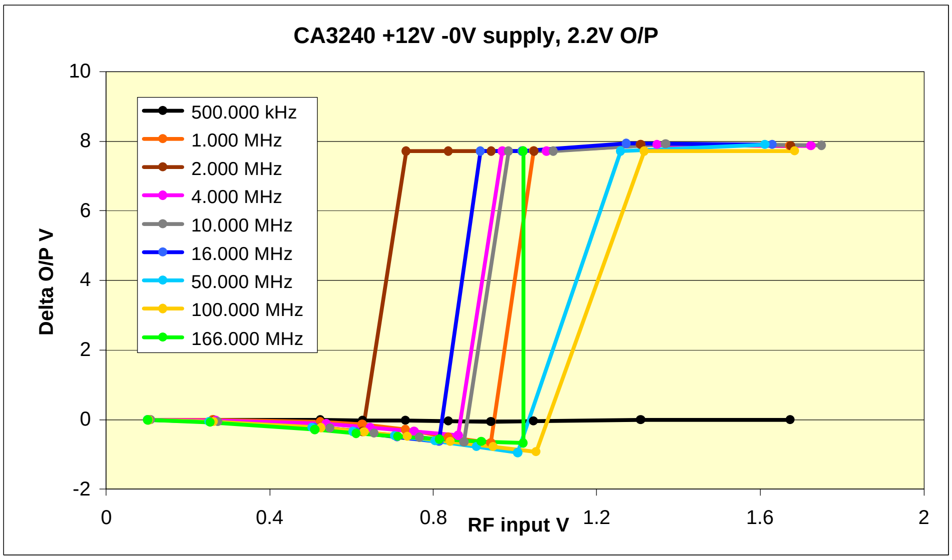






Interference transfer functions versus level (continued)





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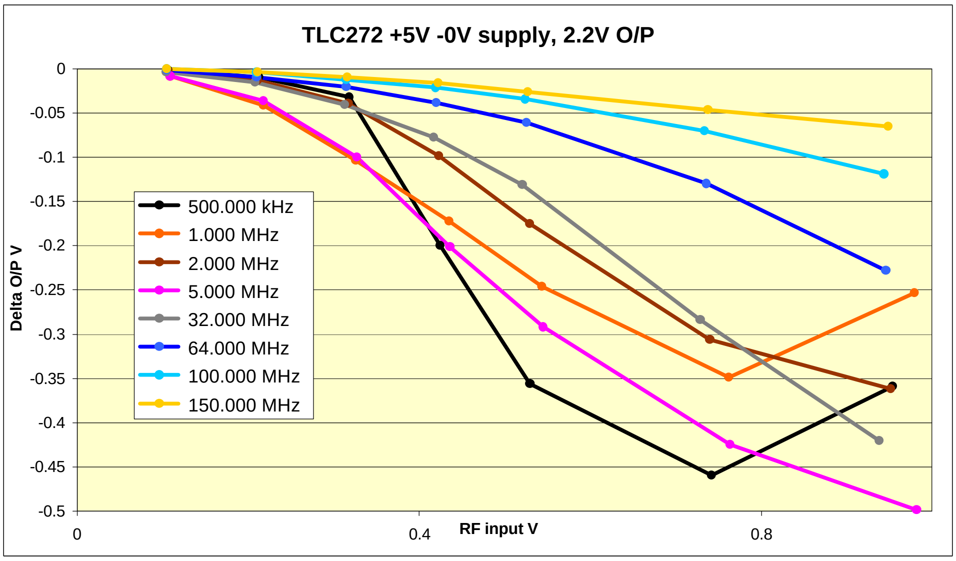
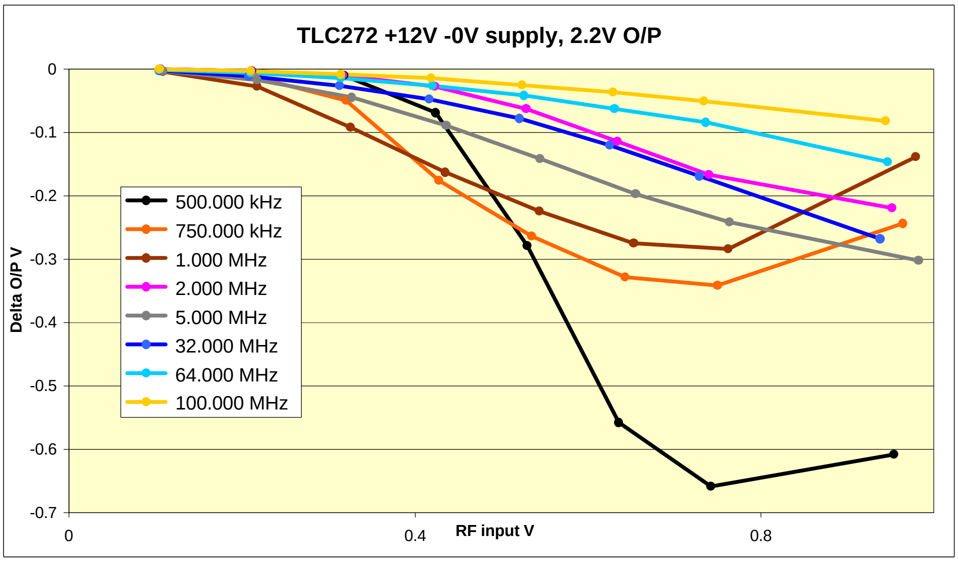
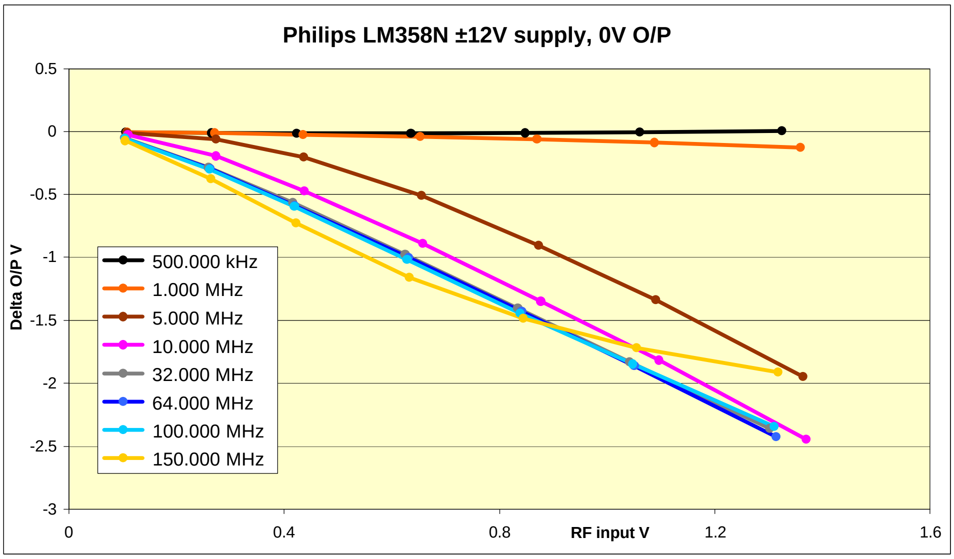
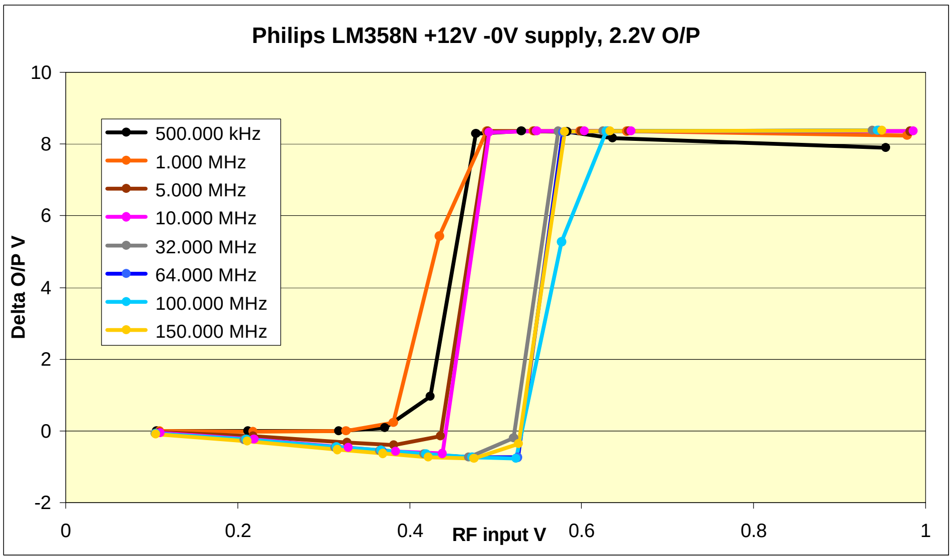
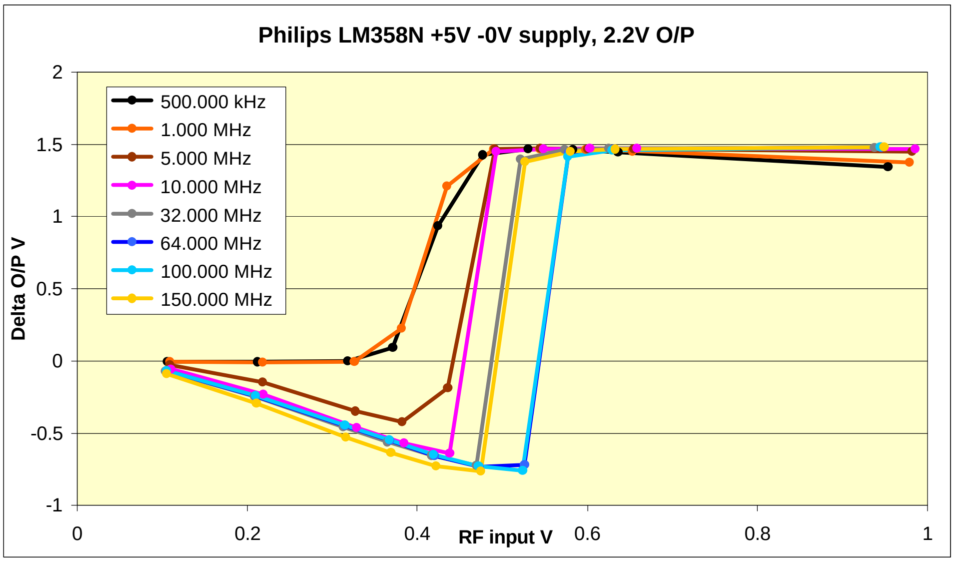




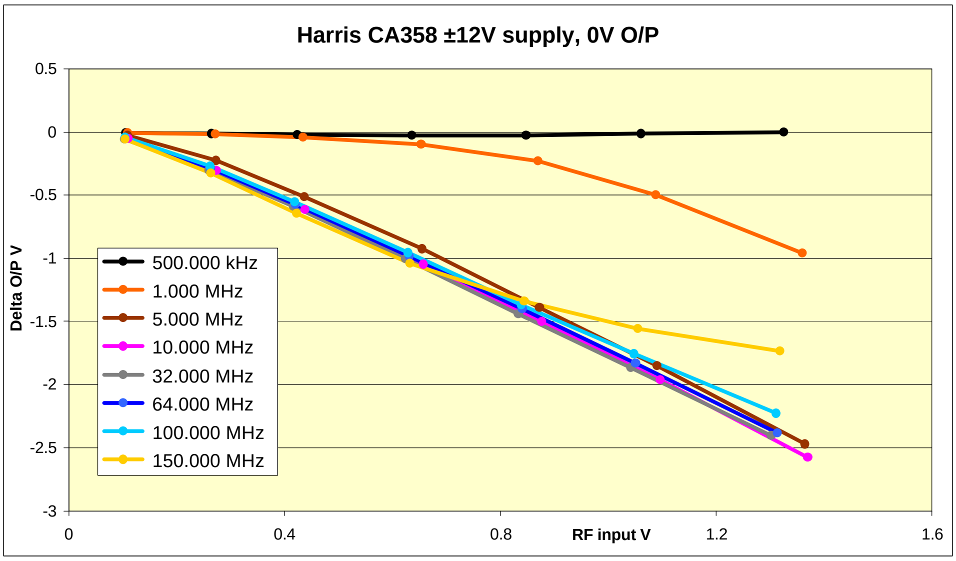
Interference transfer functions versus level (continued)

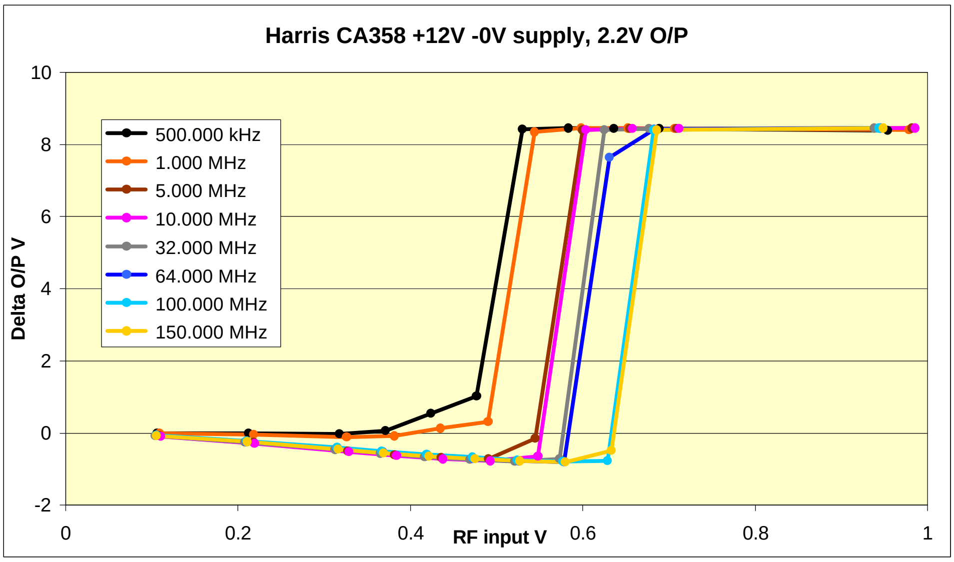


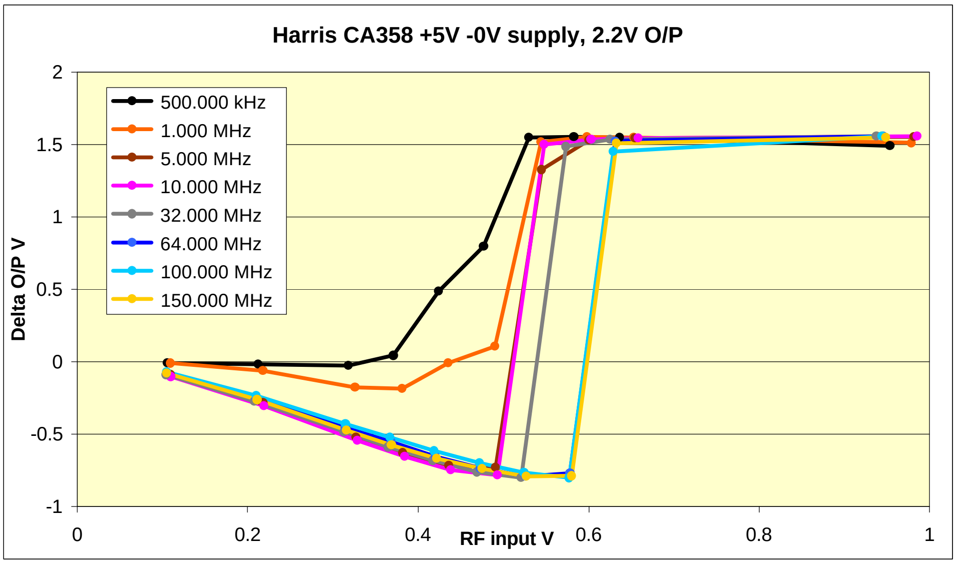




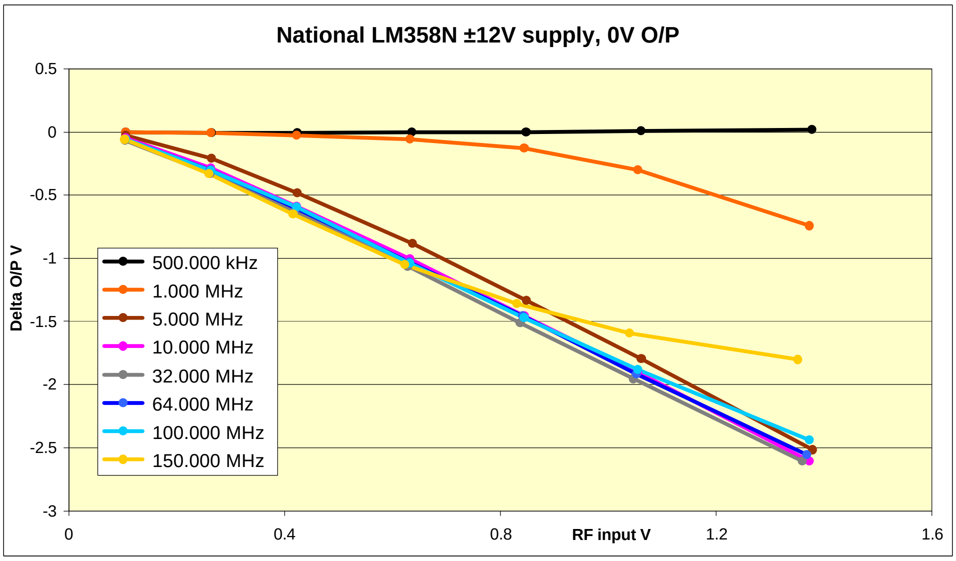
Interference transfer functions versus level (continued)

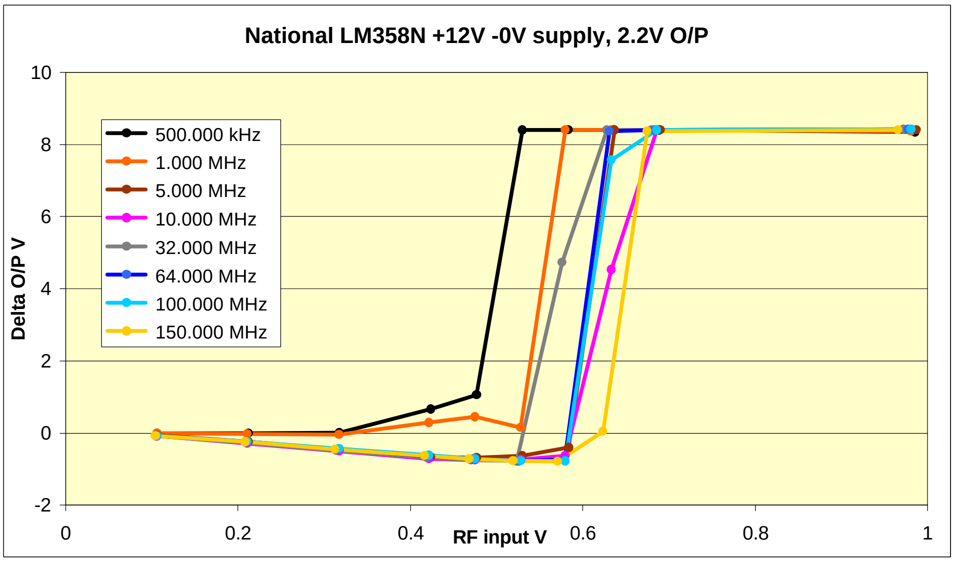


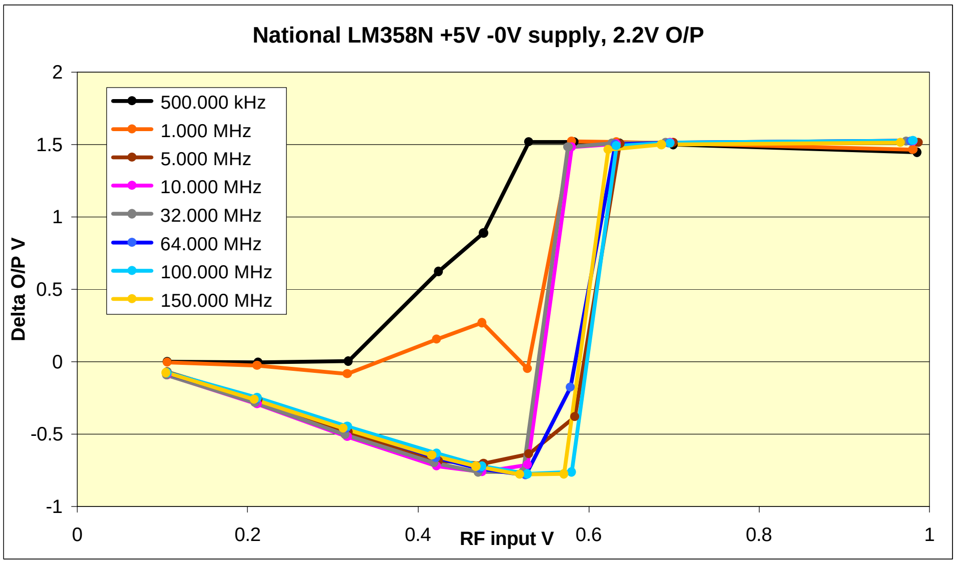




Interference transfer functions versus level (continued)



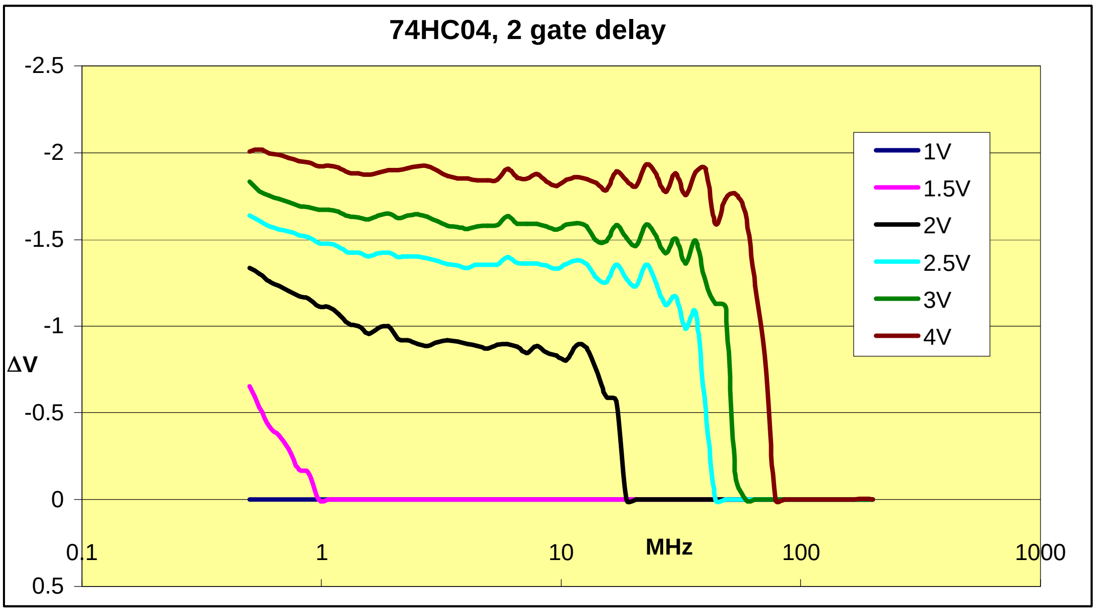


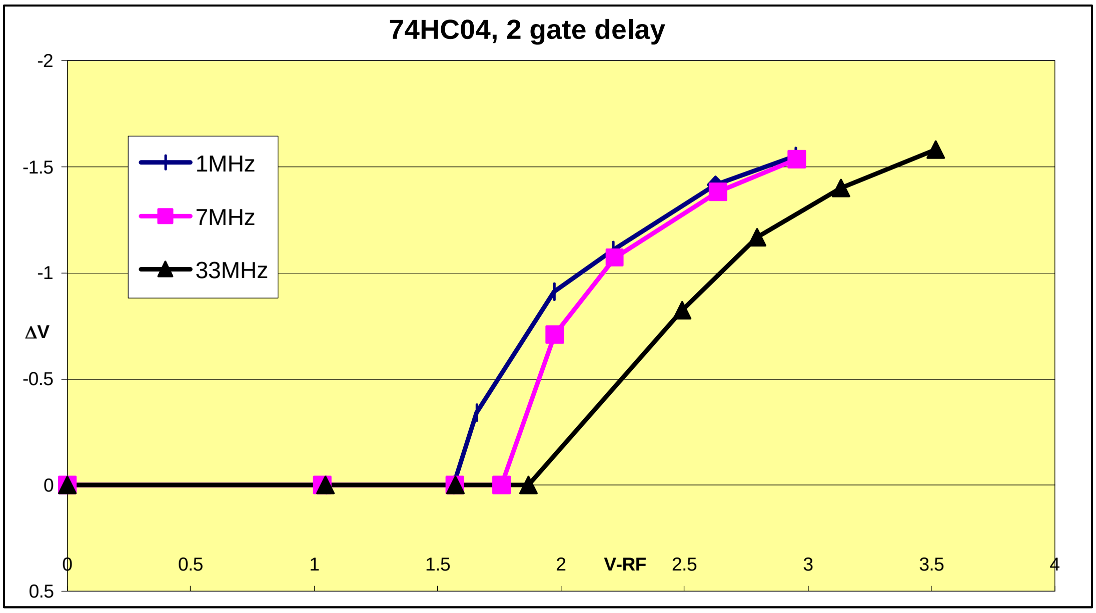


Digital circuit RF susceptibility data

Swept and spot frequency, 2 gate delays

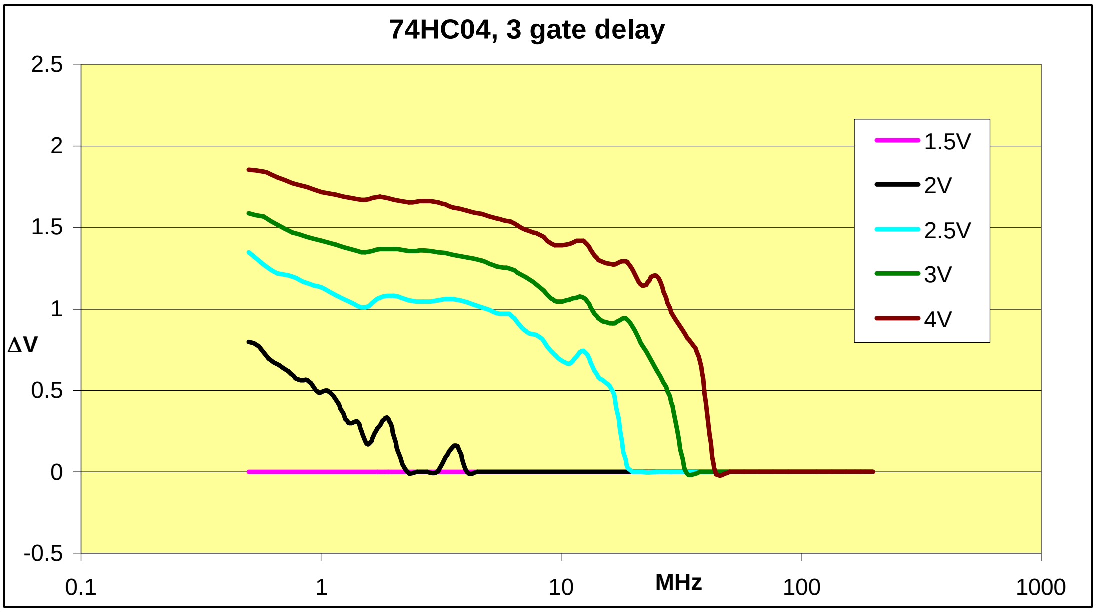
First graph shows response at six different RF levels; second graph shows response at three spot frequencies

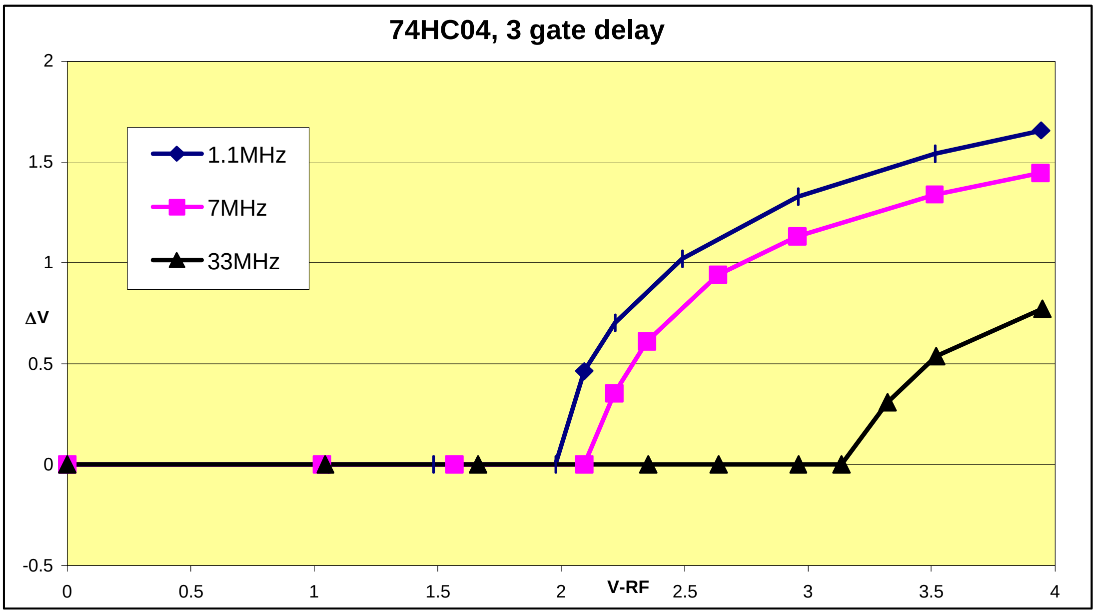




Swept and spot frequency, 3 gate delays

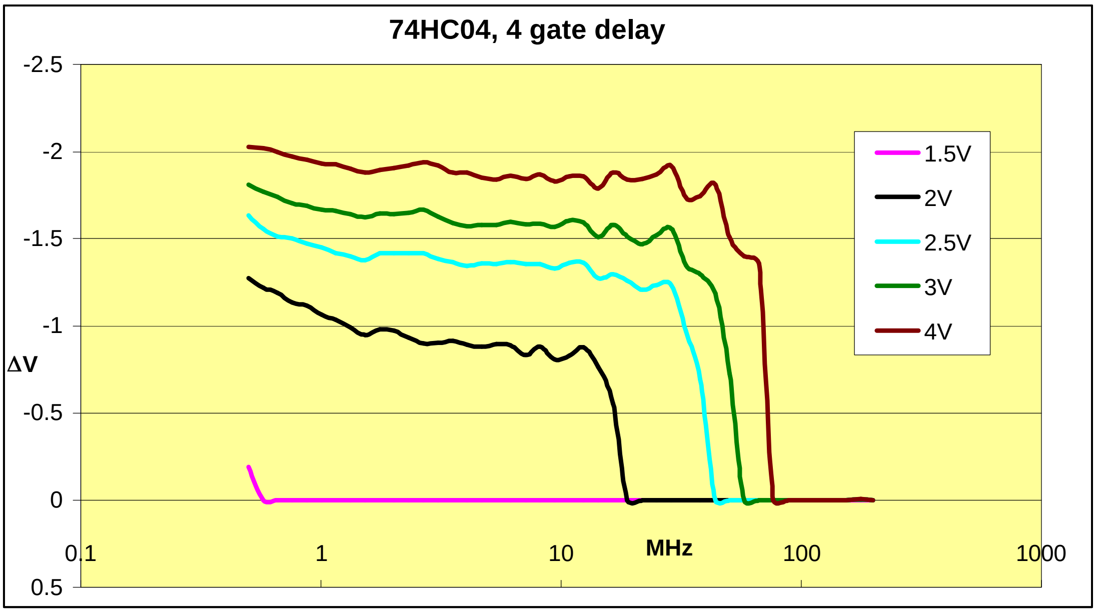
First graph shows response at five different RF levels; second graph shows response at three spot frequencies

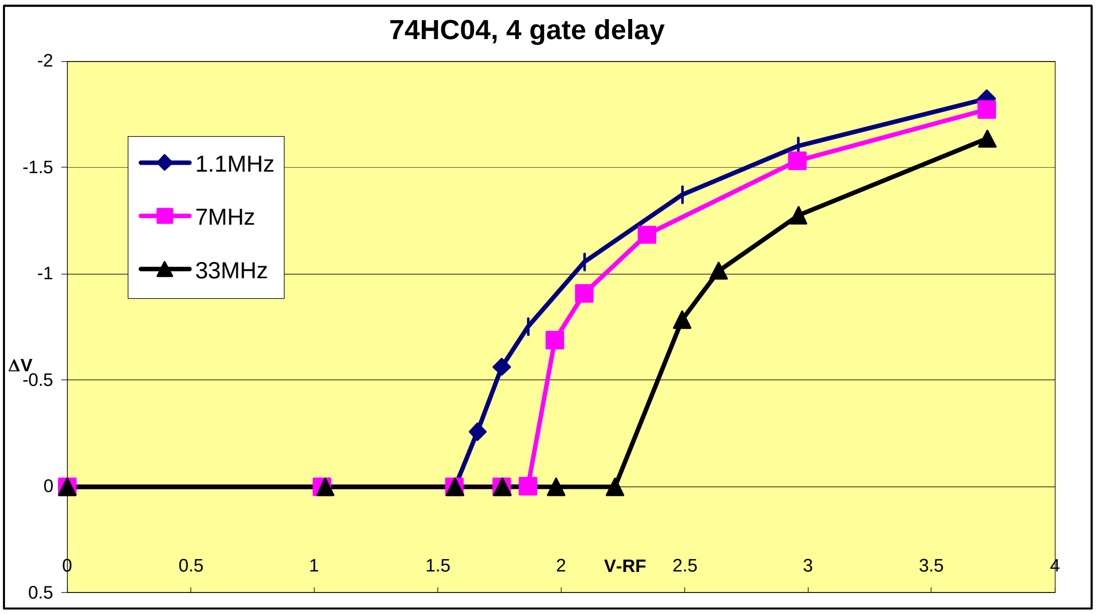




Swept and spot frequency, 4 gate delays

First graph shows response at five different RF levels; second graph shows response at three spot frequencies





Swept and spot frequency, 5 gate delays

First graph shows response at five different RF levels; second graph shows response at three spot frequencies